REMARKS

Claims 4-10 and 14-20 are in the application, with Claims 4, 5, 8, 14, 15 and 18 having been amended, and with Claims 1-3, 11-13 and 21-23 having been cancelled. Claims 4 and 14 are the independent claims herein. No new matter has been added. Reconsideration and further examination are respectfully requested.

Claim Rejections – 35 USC § 102(e)

Claims 4-10 and 14-20 are rejected as being anticipated by Box (U.S. published patent application no. 2004/0243908).

Claim 4 has been rewritten in independent form and has been substantially changed in scope. To highlight significant features now present in claim 4, the claim now recites that the instruction decoder controls the ACS engine to perform a first Viterbi decoding mode if a first instruction is received, to perform a second Viterbi decoding mode if a second instruction is received, and to perform turbo decoding if a third instruction is received. Moreover, claim 4 now recites that in the first Viterbi decoding mode, path metrics are updated from accumulators, and in the second Viterbi decoding mode, path metrics are updated from memory.

Support for the two Viterbi decoding modes and for the updating of path metrics from accumulators in one of the two modes and from memory in the other mode is found at page 6, lines 3-9 of the specification of this application.

It is noted that the Box reference does not disclose a decoder operable in the two Viterbi decoding modes now recited in claim 4, in addition to being operable for turbo decoding. It is therefore submitted that the rejection of claim 4 has now been overcome.

The above remarks are also applicable to claim 14, which has been amended in the same fashion as claim 4. The other pending claims are submitted as patentable on the same basis as their parent independent claims.[1]

[1] Applicants respectfully question the Examiner's treatment of some of the dependent claims. For example, in the case of claim 6, while FIG. 2 of the reference shows butterfly unit 16 receiving a total of 48 bits of input, it does not appear that the reference shows an accumulator having 8 units for storing 48 bits each.

As to claim 7, the reference does not appear to disclose including 16 guard bits in each of the accumulator units.

As to claim 9, the reference does not appear to disclose that a final add of a butterfly operation takes two operands if Viterbi decoding is being performed and three operands if turbo decoding is being performed.

As to claim 10, the reference does not appear to disclose looking up an operand from a look up table for the three operand add.

CONCLUSION

Accordingly, Applicants respectfully request allowance of the pending claims. If any issues remain, or if the Examiner has any further suggestions for expediting allowance of the present application, the Examiner is kindly invited to contact the undersigned via telephone at (203) 972-3460.

Respectfully submitted,

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